2000.108300
DE0340

Application for United States Letters Patent

for

METHOD OF PLATING A SEMICONDUCTOR STRUCTURE

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EXPRESS MAIL MAILING LABEL

NUMBER: EV 291396037 US

DATE OF DEPOSIT: July 29, 2003

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METHOD OF PLATING A SEMICONDUCTOR STRUCTURE

BACKGROUND OF THE INVENTION

1. FIELD OF THE INVENTION

The present invention relates to the field of manufacturing of integrated circuits, and, more particularly, to the deposition of metal layers on semiconductor structures.

2. DESCRIPTION OF THE RELATED ART

Integrated circuits comprise a large number of individual circuit elements, such as transistors, capacitors and resistors, formed on a semiconductor substrate. The circuit elements are internally connected by means of metal lines to form complex circuits, like memory devices, logic devices and microprocessors.

In modern integrated circuits, these metal lines are frequently formed by means of a so-called damascene process, wherein, on a semiconductor substrate, an interlayer dielectric is deposited in which vias and trenches are formed. These vias and trenches are then filled with metal, *e.g.*, copper, to provide electrical contact between the circuit elements. To this end, a metal layer is deposited. In the following, the metal used for filling the vias and trenches will be denoted as "conductor metal."

Frequently, electroplating is used for the deposition of a conductor metal layer comprised of copper. Electroplating is an electrochemical process which can be performed in specialized plating cells.

A plating cell according to the state of the art is described with reference to Figure 1. A plating cell 100 comprises a container 101, which is adapted to receive an electrolyte 102. An electrode 103, which is substantially comprised of the conductor metal, is provided within the container 101. The plating cell 100 further comprises a substrate holder 104 provided partially within the container 101 and being adapted to receive a semiconductor structure 105. The semiconductor structure 105 typically has a relatively thin conductive seed layer, such as, for example, a copper seed layer, formed above the surface of an insulating layer formed on the substrate. A contact ring 106 provides electrical contact between the semiconductor structure 105 and the substrate holder 104. The electrode 103 and the substrate holder 104 are electrically connected to a power source 109, which is connected to a control unit 110.

In operation, the electrode 103 and the semiconductor structure 105 are in contact with the electrolyte 102. The electrolyte 102 comprises ions of a conductor metal. If the conductor metal is copper, the electrolyte may be, *e.g.*, an aqueous solution of copper sulfate comprising Cu^{2+} and SO_4^{2-} ions. The control unit 110 controls the power source 109 to apply a current between the electrode 103 and the substrate holder 104. A polarity of this current is such that the electrode 103 becomes an anode and the semiconductor structure 105 becomes a cathode. At the electrode 103, atoms of the conductor metal are positively ionized and change from a solid state in the electrode 103 into a solvent state in the electrolyte 102. At the semiconductor structure 105, positively charged ions of the conductor metal are discharged and change from the solvent state in the electrolyte to the solid state. In the course of time, a metal layer 107 comprising the conductor metal is deposited on the surface of the semiconductor structure 105.

As a further step of the damascene technique, a chemical mechanical polishing process is performed to remove excess metal deposited during the previous plating process to reliably fill the vias and trenches. In chemical mechanical polishing, the semiconductor structure 105 is moved relative to a polishing pad. Slurry is supplied to an interface between the semiconductor structure 105 and the polishing pad. The slurry comprises a chemical compound reacting with the material or materials on the surface of the semiconductor structure 105. The reaction product is removed by abrasives contained in the slurry and/or the polishing pad. Thereby, the conductor metal is removed from elevations between the vias and trenches and the surface of the semiconductor structure 105 is planarized.

The damascene process is explained in more detail with reference to Figures 2a-2c. Figure 2a shows a schematic cross-sectional view of a semiconductor structure 200. In an interlayer dielectric 201, a trench 204 and vias 205, 206 are formed. In the following, portions 210-213 adjacent the trench 204 and the vias 205, 206 are denoted as "elevations." A barrier layer 202 is formed on the interlayer dielectric 201. The barrier layer 202 inhibits a diffusion of conductor metal into the interlayer dielectric 201 and increases the adhesive strength between the conductor metal and the interlayer dielectric 201. The semiconductor structure 200 further comprises a seed layer 203 containing the conductor metal. In electroplating, the seed layer 203 improves the conductivity of the semiconductor structure 200. The seed layer 203 and the barrier layer 202 may be formed using methods known in the art, such as chemical vapor deposition (CVD) and physical vapor deposition (PVD).

Figure 2b shows a schematic cross-sectional view of the semiconductor structure 200 after the electroplating process. A metal layer 207 has been formed on the surface of the semiconductor structure 200. Typically, electroplating is performed under conditions where

growth of the metal layer 207 starts at the bottom of narrow recesses like vias 205, 206 and rapidly progresses upwards. This may be effected by adding specialized additives to the electrolyte and/or by applying a pulsed current between the electrode and the semiconductor structure 200. In a wide recess-like trench 204, the metal layer 207 grows slower than in the vias 205, 206. In order to completely fill the trench 204 with conductor metal, electroplating must be continued after the filling of the vias 205, 206. In doing so, the metal layer 207 grows to a thickness d over the elevations 210-213 and the vias 205, 206. This is denoted as "overdeposition."

Figure 2c shows the semiconductor structure 200 after the chemical mechanical polishing process. Portions of the metal layer 207, portions of the seed layer 203 and portions of the barrier layer 202 have been removed to expose the elevations 210-213.

In summary, in conventional damascene processes, electroplating is performed under overdeposition conditions where excess metal is deposited on elevations of the semiconductor structure in order to ensure that wide recesses are filled with metal. This excess metal is removed in a subsequent chemical mechanical polishing process.

A problem with conventional damascene processes is that a large volume of waste slurry that may be harmful to the environment is created while the excess metal is removed by means of chemical mechanical polishing. Another problem with conventional damascene processes is that long process times are required for the chemical mechanical polishing process, leading to high operation costs. Yet another problem with conventional damascene processes is that highly sophisticated chemical mechanical polishing technology must be developed and maintained. Yet another problem with conventional damascene processes is

that semiconductor structures may be scratched in the chemical mechanical polishing process. Yet another problem with conventional damascene processes is that mechanical load in the chemical mechanical polishing process may damage the interlayer dielectric, in particular if comparatively soft materials having a low dielectric constant are used.

In view of the above-mentioned problems, a need exists for a method of depositing a metal layer on a semiconductor structure with reduced overdeposition. The present invention is directed to various methods and systems that may solve or reduce one or more of the problems identified above.

SUMMARY OF THE INVENTION

The present invention is generally directed to a method of depositing a metal layer on a semiconductor structure where a metal layer is deposited by means of electroplating and the metal layer is subsequently smoothed in an electropolishing process.

According to an illustrative embodiment of the present invention, a method of forming a layer of metal on a semiconductor structure comprises bringing an electrode into contact with an electrolyte and bringing the semiconductor structure into contact with the electrolyte. In a first time interval, a first current flowing from the electrode through the electrolyte to the semiconductor structure is applied. The first current has a first amperage comprising a plurality of first positive pulses and a plurality of first negative pulses. An integral of the first amperage over the first time interval has a first value greater than zero. In a second time interval, a second current flowing from the electrode through the electrolyte to the semiconductor structure is applied. The second current has a second amperage. An integral of the second amperage over the second time interval has a second value less than zero.

According to another illustrative embodiment of the present invention, a method comprises providing a semiconductor structure comprising at least one recess and at least one elevation. The semiconductor structure is subjected to an electroplating process to deposit a layer of metal on the semiconductor structure and to fill the recess with the metal. The semiconductor structure is electropolished for preferentially removing the metal from the elevation. The method further comprises chemical mechanical polishing the semiconductor structure. The chemical mechanical polishing removes a surplus of the metal from the elevation and planarizes a surface of the semiconductor structure.

According to yet another illustrative embodiment of the present invention, a plating cell for depositing a layer of metal on a semiconductor structure comprises a container being adapted to receive an electrolyte. An electrode is provided at least partially within the container. A substrate holder is adapted to receive the semiconductor structure and to provide electrical contact to the semiconductor structure. The substrate holder is provided at least partially within the container. A power source is electrically connected to the electrode and to the substrate holder. The plating cell also comprises a control unit being adapted to control the power source to apply in a first time interval a first current flowing from the electrode through the electrolyte to the semiconductor structure. The first current has a first amperage comprising a plurality of first positive pulses and a plurality of first negative pulses. An integral of the first amperage over the first time interval has a first value greater than zero. The control unit is further adapted to control the power source to apply in a second time interval a second current flowing from the electrode through the electrolyte to the semiconductor structure. The second current has a second amperage. An integral of the second amperage over the second time interval has a second value less than zero.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention may be understood by reference to the following description taken in conjunction with the accompanying drawings, in which like reference numerals identify like elements, and in which:

Figure 1 shows a sketch of an illustrative prior art plating cell for electroplating;

Figures 2a-2c show schematic cross-sectional views of a semiconductor structure in subsequent stages of a prior art damascene process;

Figure 3 shows the time dependence of an amperage of a current between an electrode and a semiconductor structure in a method according to an embodiment of the present invention;

Figure 4 shows a schematic cross-sectional view of a semiconductor structure in a stage of a method according to an embodiment of the present invention;

Figures 5a-5b show the time dependence of an amperage of a current between an electrode and a semiconductor structure in electroplating processes in methods according to embodiments of the present invention; and

Figures 6a-6b show the time dependence of an amperage of a current between an electrode and a semiconductor structure in electropolishing processes in methods according to embodiments of the present invention.

While the invention is susceptible to various modifications and alternative forms, specific embodiments thereof have been shown by way of example in the drawings and are herein described in detail. It should be understood, however, that the description herein of specific embodiments is not intended to limit the invention to the particular forms disclosed, but on the contrary, the intention is to cover all modifications, equivalents, and alternatives falling within the spirit and scope of the invention as defined by the appended claims.

DETAILED DESCRIPTION OF THE INVENTION

Illustrative embodiments of the invention are described below. In the interest of clarity, not all features of an actual implementation are described in this specification. It will of course be appreciated that in the development of any such actual embodiment, numerous implementation-specific decisions must be made to achieve the developers' specific goals, such as compliance with system-related and business-related constraints, which will vary from one implementation to another. Moreover, it will be appreciated that such a development effort might be complex and time-consuming, but would nevertheless be a routine undertaking for those of ordinary skill in the art having the benefit of this disclosure.

The present invention will now be described with reference to the attached figures. Although the various regions and structures of a semiconductor device are depicted in the drawings as having very precise, sharp configurations and profiles, those skilled in the art recognize that, in reality, these regions and structures are not as precise as indicated in the drawings. Additionally, the relative sizes of the various features and doped regions depicted in the drawings may be exaggerated or reduced as compared to the size of those features or regions on fabricated devices. Nevertheless, the attached drawings are included to describe

and explain illustrative examples of the present invention. The words and phrases used herein should be understood and interpreted to have a meaning consistent with the understanding of those words and phrases by those skilled in the relevant art. No special definition of a term or phrase, *i.e.*, a definition that is different from the ordinary and customary meaning as understood by those skilled in the art, is intended to be implied by consistent usage of the term or phrase herein. To the extent that a term or phrase is intended to have a special meaning, *i.e.*, a meaning other than that understood by skilled artisans, such a special definition will be expressly set forth in the specification in a definitional manner that directly and unequivocally provides the special definition for the term or phrase.

The present invention allows the deposition of a metal layer to fill recesses on a semiconductor structure with reduced overdeposition. The semiconductor structure is electroplated to form a layer of metal which fills recesses like trenches and vias. Then, the semiconductor structure is electropolished. Electropolishing preferentially removes metal from elevations of the semiconductor structure. This effect may be used to advantageously reduce the thickness of the metal layer over the elevations, while the recesses remain filled with metal. In a subsequent chemical mechanical polishing process, only a thin metal layer must be removed to expose the elevations. Thus, the demands on chemical mechanical polishing and potential adverse effects of chemical mechanical polishing to the semiconductor structure may be reduced significantly.

In embodiments of the present invention, a method of forming a layer of metal on a semiconductor substrate is performed in a plating cell, as shown in Figure 1. A semiconductor structure 105 is provided. In particular embodiments of the present invention, the semiconductor structure 105 is a wafer comprising a plurality of circuit elements, such as

transistors, capacitors and resistors. On top of the circuit elements, an interlayer dielectric is deposited which may comprise silicon dioxide (SiO_2) or a material having a low dielectric constant like silicon oxyfluoride, hydrogenated silsesquioxane or fluorinated polyimide. The interlayer dielectric is patterned by etching vias and trenches. Vias can be provided at the bottom of a trench. After the completion of the damascene process, these vias are filled with metal and provide electrical contact between a metal line formed in the trench and a circuit element below the trench. On the interlayer dielectric, a barrier layer comprising, *e.g.*, tantalum, tantalum nitride, titanium or titanium nitride and an electrically conductive seed layer are formed. The seed layer may comprise the conductor metal. The formation of these layers may be performed using known methods like chemical vapor deposition or physical vapor deposition. Alternatively, the seed layer can be formed by means of electroless deposition.

An electrode 103 comprising the conductor metal is brought into contact with an electrolyte 102. This can be done by immersing the electrode 103 into an electrolyte bath, in particular by providing the electrode 103 in a container 101 which is filled with the electrolyte 102.

In other embodiments, the electrode 103 is immersed only partially into the electrolyte 102. The electrode 103 can protrude from a surface of the electrolyte 102 or may be integrated into a wall of the container 101. However, any other configuration of presently available plating tools or future tool generations may also be used.

The conductor metal can comprise copper. In other embodiments, the conductor metal may comprise aluminum, tungsten, or a noble metal like gold, silver or platinum. The

electrolyte 102 comprises ions of the conductor metal. Usually, solved metal ions are positively charged. In particular, the electrolyte 102 may comprise a solution of a sulfate, a halogenide (*e.g.*, a chloride), a hydroxide or a cyanide of the conductor metal. If the conductor metal is copper, the electrolyte 102 may comprise an aqueous solution of copper sulfate ($CuSO_4$), which dissociates into Cu^{2+} ions and SO_4^{2-} ions. The electrolyte 102 may also comprise an acid increasing its conductivity, *e.g.*, sulfuric acid (H_2SO_4). The electrolyte may comprise additives like a polyether, *e.g.*, DAG polymer or polyalkylene glycol, and/or an organic sulfide, *e.g.*, Bis(3-sulfopropyl)-disodium-sulfonate and/or a nitrogen compound and/or polyethylenglycole and/or polypropylenglycole and/or polymer phenazonium derivates and/or dithiocarbaminacid derivates.

The semiconductor substrate 105 is fixed to a substrate holder 104. An electrically conductive contact ring 106 may be used to provide electrical contact between the seed layer and the substrate holder 104. Subsequently, the semiconductor substrate 105 is brought into contact with the electrolyte 102. This can be done by moving the substrate holder 104 towards the surface of the electrolyte 102 until the semiconductor structure 105 is at least partially immersed into the electrolyte 102. The semiconductor structure 105 may be held close to the electrolyte surface such that only the patterned surface of the semiconductor structure 105 is wetted by the electrolyte 102 whereas its reverse side remains dry. In other embodiments, the semiconductor structure 105 can be totally immersed into the electrolyte 102.

A current is applied between the electrode 103 and the semiconductor structure 105. This can be done by controlling a power source 109 being connected to the electrode 103 and the semiconductor structure 105. The current flows in a current direction from the power

source 109 to the electrode 103, from the electrode 103 through the electrolyte 102 to the semiconductor structure 105, and from the semiconductor structure 105 via the substrate holder 104 back to the power source 109. The current has an amperage I(t), which may vary as a function of time t. The amperage I(t) may be zero, greater than zero (positive) or less than zero (negative). Since we have defined the current direction as the direction from the electrode 103 to the semiconductor structure 105, if the amperage I(t) is positive, the electrode 103 is an anode, the semiconductor structure 105 is a cathode, and positively charged ions (*e.g.*, metal ions) in the electrolyte move toward the semiconductor structure 105. Conversely, if the amperage I(t) is negative, the semiconductor structure 105 is an anode, the electrode 103 is a cathode, and positively charged ions move away from the semiconductor structure 105. According to Faraday's law, in an infinitesimal time interval dt, a mass

$$dM = I(t)dt\frac{m}{nF} \qquad (1)$$

of the conductor metal is transported from the electrode 103 to the semiconductor structure 105. $F = 4.6487 \times 10^4$ As/mol is Faraday's constant, M is a molar mass of the conductor metal, and n is a number of electrons needed to discharge an ion of the conductor metal. Consequently, in a time interval from $t = \tau_1$ to $t = \tau_2$, a mass

$$M = \frac{m}{nF}\int_{\tau_1}^{\tau_2} I(t)dt \qquad (2)$$

is transported. If the integral of the amperage I(t) on the right hand side of equation (2) has a value greater than zero, m is positive. Consequently, in the time interval from τ_1 to τ_2,

conductor metal is deposited on the semiconductor structure. This is the case if an electroplating process is performed. Conversely, if the integral has a value less than zero, in the time interval from τ_1 to τ_2, conductor metal is removed from the semiconductor structure 105 and transported towards the electrode 103. This process is denoted as "electropolishing."

Figure 3 shows the dependence of the current I(t) on time t in a method according to an embodiment of the present invention. In a first time interval from $t = t_o$ to $t = t_1$, an electroplating process is performed. The current applied in the first time interval (denoted as "first current" in the following) has an amperage comprising a plurality of first positive pulses 301-304 and a plurality of first negative pulses 305-308. Each first positive pulse is followed by a first negative pulse.

A positive pulse is created by applying a current having a positive amperage for a short time. Conversely, a negative pulse is created by applying a current having a negative amperage for a short time. It is to be noted that the number of pulses shown in the figures of the present application is merely illustrative; in practice, the number of applied pulses can be much greater.

In the embodiment described with reference to Figure 3, in each of the first positive pulses 301-304, a current having an amperage I_1 greater than zero is applied for a time θ_1. In each of the first negative pulses 305-308, a current having an amperage I_2 less than zero is applied for a time θ_2. Thus, the first positive pulses and the first negative pulses have a substantially rectangular shape. If a number N_1 of positive and negative pulses is applied, an integral of the amperage I(t) of the first current over the first time interval has a first value N_1

($I_1\theta_1 + I_2\theta_2$). In an electroplating process, this first value must be positive, which corresponds to the condition $|I_1|\ \theta_1 > |I_2|\ \theta_2$.

The first positive pulses 301-304 can have an amperage I_1 of about 4 amperes to about 10 amperes and may be applied for a time θ_1 of about 60 milliseconds to about 120 milliseconds. The first negative pulses can have an amperage I_2 of about 2 amperes to about 6 amperes and may be applied for a time θ_2 of about 5 milliseconds to about 30 milliseconds. The number N_1 of first positive and first negative pulses can be about several thousand pulses. The first time interval may have a duration of about one minute to about five minutes.

In other embodiments of the present invention, both the individual positive pulses and the individual negative pulses may have different amperages and the durations of the individual pulses may be different. The number of first positive and first negative pulses need not be equal. A first positive pulse may be followed by a plurality of first negative pulses. Alternatively, a first negative pulse may be followed by a plurality of first positive pulses.

After the electroplating process, in a second time interval from t_2 to t_3, an electropolishing process is performed. In the embodiment described with reference to Figure 3, an amperage of a current applied in the second time interval (denoted as "second current" in the following) comprises a plurality of second negative pulses 309-313. In one embodiment, each of the second negative pulses 309-313 has a duration θ_3 and an amperage I_3 less than zero. If a number N_3 of second negative pulses is applied in the second time interval, an integral of the amperage of the second current over the second time interval has a second

value $N_3I_3\theta_3$. Since the second value is less than zero, conductor metal is removed from the semiconductor structure 105. Preferably, an absolute of the first value is greater than an absolute of the second value, such that a part of the conductor metal remains on the semiconductor structure 105.

The second time interval may have a duration of more than thirty seconds. The second negative pulses may have a duration θ_3 of about one millisecond to about 30 milliseconds and an amperage I_3 of about 6 amperes to about 15 amperes. The number N_3 of second negative pulses may be about 1000.

The features of a metal film deposited by means of a method according to an embodiment of the present invention are described with reference to Figure 4. Figure 4 shows a schematic cross-sectional view of a semiconductor structure 400 which comprises a trench 404 and vias 405, 406 formed in an interlayer dielectric 401. A barrier layer 402 and a seed layer 403 are formed on the interlayer dielectric 401. In the electroplating process, a metal layer 407 is deposited. Thereby, the trench 404 and the vias 405, 406 are filled with conductor metal. The dashed line 409 schematically shows the extension of the metal layer 407 after the electroplating process. Since there is overdeposition, the metal layer 407 on elevations 410-413 between the trench 404 and the vias 405, 406 has a thickness d.

In the electropolishing process, a portion 408 of the metal layer 407 is removed. Metal is preferentially removed from the elevations 410-413, while the removal of material in portions of the metal layer 407 above the trench 404 occurs at a lower rate. This effect is believed to be due to the fact that the electric field is strongest where the distance between the electrode and the surface of the metal layer 407 is minimal, which is the case in the elevated

portions 410-413 of the semiconductor structure 400. Where the electric field is strongest, the current density is also strongest, resulting in the highest removal rate in that area.

Above the elevations 410-413 and the narrow vias 405, 406, a portion of the metal layer 407 having a thickness Δd_1 is removed. Above the trench 404, a portion of the metal layer 407 having a thickness Δd_2 being less than the thickness Δd_1 is removed. Thus, the electropolishing process smoothens the surface of the metal layer 407. If, after electropolishing, the amount of metal remaining in the trench 404 is just sufficient to fill the trench 404, the thickness of a metal layer left on the elevations 410-413 of the semiconductor structure 400 is considerably smaller than in a conventional damascene process.

Subsequently, the semiconductor structure 105, 400 is removed from the plating cell 100 and a chemical mechanical polishing process is performed. Thereby, a surplus of the metal layer 407 and portions of the seed layer 403 and the barrier layer 402 are removed from the elevations 410-413, the elevations 410-413 are exposed and the surface of the semiconductor structure 400 is planarized. Thus, a semiconductor structure similar to that shown in Figure 2c is obtained.

Since the thickness of the metal layer that must be removed from the elevations of the semiconductor structure is smaller than in a damascene process according to the state of the art, the demands on the chemical mechanical polishing process in a method according to the present invention are significantly reduced. Thus, the cost of operation of a chemical mechanical polishing device and the risk of adverse effects of chemical mechanical polishing to the semiconductor structure are advantageously minimized.

Figure 5a shows an amperage $I_{f,a}(t)$ of a first current applied in a first time interval from $t = t_0$ to $t = t_1$ where electroplating is performed in a method according to another embodiment of the present invention. The amperage $I_{f,a}(t)$ comprises a plurality of positive pulses 501-508. Each pulse has an amperage I_4 greater than zero and a duration θ_4. If a number N_4 of positive pulses is applied in the first time interval, an integral of the amperage $I_{f,a}(t)$ of the first current over the first time interval has a value $N_4 I_4 \theta_4$. In other embodiments of the present invention, the individual positive pulses 501-508 may have different amperages and/or different durations.

Figure 5b shows an amperage $I_{f,b}(t)$ of a first current applied in a first time interval from $t = t_0$ to $t = t_1$ where electroplating is performed in a method according to a further embodiment of the present invention. The amperage $I_{f,b}(t)$ depends on time t like

$$A_1 \sin(\omega_1 t + \phi_1) + B_1.$$

Here, A_1 is an amplitude of an AC component of the current, ω_1 is an angular frequency of the AC component, φ_1 is a phase shift and B_1 is an offset greater than zero. An absolute of the amperage A_1 is greater than the offset B_1. Therefore, the amperage $I_{f,b}(t)$ comprises both positive pulses 509-512 and negative pulses 513-515.

In other embodiments, the absolute of the amplitude A_1 may be equal to the offset B_1. Thus, the amperage $I_{f,b}(t)$ comprises only positive pulses. The absolute of the amplitude A_1 may also be smaller than the offset B_1 such that the amperage $I_{f,b}(t)$ is always positive during the first time interval.

Figure 6a shows an amperage $I_{s,a}(t)$ of a second current in a second time interval from $t = t_2$ to $t = t_3$ where electropolishing is performed in a method according to a further embodiment of the present invention. The amperage $I_{s,a}(t)$ comprises a plurality of negative pulses 601-604 and a plurality of positive pulses 605-608. Each positive pulse is followed by a negative pulse. The negative pulses 601-604 have an amperage I_5 less than zero and a duration θ_5. The positive pulses have an amperage I_6 greater than zero and a duration θ_6. If a number N_6 of positive and negative pulses is applied, an integral of the amperage $I_{s,a}(t)$ over the second time interval has a value $N_6(I_6\theta_6+I_5\theta_5)$. In electropolishing, this value must be less than zero, which is the case if $|I_6|\theta_6 > |I_5|\theta_5$.

Figure 6b shows an amperage $I_{s,b}(t)$ of a second current applied in a second time interval from t_2 to t_3 where electropolishing is performed in a method according to a further embodiment of the present invention. The amperage $I_{s,b}(t)$ has a sinusoidal time dependence,

$$A_2 \sin(\omega_2 t + \phi_2) + B_2,$$

where A_2 is an amplitude of an AC component of the current, ω_2 is an angular frequency, and φ_2 is a phase shift. B_2 is an offset less than zero. An absolute of the offset B_2 equals an absolute of the amplitude A_2. Thus, the amperage $I_{s,b}(t)$ comprises a plurality of negative pulses 609-611, but no positive pulses.

In other embodiments, the absolute of the amplitude A_2 may be greater than the absolute of the offset B_2 such that the amperage $I_{s,b}(t)$ comprises positive pulses in addition to the negative pulses 609-611. Alternatively, the absolute of the amplitude A_2 may be smaller

than the absolute of the offset B_2 such that the amperage $I_{s,b}(t)$ is always positive in the second time interval.

In other embodiments, the amperage of the first current may be substantially constant and greater than zero during the first time interval, and/or the amperage of the second current may be substantially constant and less than zero during the second time interval.

In further embodiments of the present invention, a second electroplating process is performed after the electropolishing process. This can be done by applying in a third time interval a third current flowing from the electrode 103 through the electrolyte 102 to the semiconductor structure 105. An amperage of the third current can have a time dependence similar to the amperage of the first current in any of the embodiments described above. In other embodiments, durations and/or amperages of pulses and/or the shape of pulses may differ from that used in the first current. The second electroplating process may be followed by a second electropolishing process. This can be done by applying in a fourth time interval a fourth current. An amperage of the fourth current can have a time dependence similar to the amperage of the second current in the embodiments described above. In other embodiments, durations and/or amperages of pulses and/or the shape of pulses may differ from that used in the second current.

A plating cell according to an embodiment of the present invention may have an assembly as shown in Figure 1. The plating cell 100 comprises a container 101 being adapted to receive an electrolyte 102, an electrode 103 and a substrate holder 104. The substrate holder 104 is adapted to receive a semiconductor structure 105 and to provide electrical contact to the semiconductor structure 105. A contact ring 106 provides electrical

contact between the conductive seed layer formed above the semiconductor structure 105 and the substrate holder 104. A power source 109 is connected to the electrode 103 and the substrate holder 104. A control unit 110 is adapted to control the power source 109 to apply currents between the electrode 103 and the semiconductor structure 105 for depositing a metal layer 107 on the semiconductor structure 105 in an electroplating process and for smoothening the metal layer 107 in an electropolishing process. The control unit can be adapted to apply currents whose amperage has a time dependence as in the methods according to the present invention previously described.

The performance of a method according to the present invention may be influenced by process parameters like a temperature of the electrolyte, the time dependence of applied currents, in particular amperages and durations of pulses, numbers of applied pulses and angular frequencies, the geometrical arrangement of components of the plating cell, concentrations of components of the electrolyte, in particular concentrations of conductor metal ions and additives, and the conductivity of the electrolyte.

Measures for the performance of a method according to the present invention are the total process time required to deposit the metal layer, the likelihood of the formation of trapped voids filled with electrolyte in narrow vias and the roughness of the metal layer which is obtained after the electropolishing process.

The total process time may be controlled by varying amperages of currents applied in the electroplating and the electropolishing process. Reducing the total process time advantageously increases the throughput of a plating cell and reduces costs of operation of the plating cell.

Trapped voids adversely affect the conductive properties of vias filled with metal. The likelihood of the formation of trapped voids may be reduced significantly if the amperage of the first current applied in the electropolishing process comprises both positive and negative pulses, as in the embodiments described with reference to Figures 4 and 6b, and/or by adding additives to the electrolyte. Thus, the likelihood of a failure of interconnects in the completed semiconductor structure may be advantageously reduced.

Reducing the roughness of the metal layer obtained at the end of the electropolishing process advantageously reduces the amount of conductor metal that must be removed in chemical mechanical polishing. Empirically it has been shown that applying a current comprising negative pulses in the second time interval where electropolishing is formed, as in the embodiments described with reference to Figures 4, 6a and 6b, leads to an effective removal of excess metal in regions above the elevations of the semiconductor structure.

Embodiments of the present invention may include an optimization of the process parameters. Test structures comprising vias and/or trenches of various diameters and depths may be used to study the effects of a variation of the process parameters on the performance of the method according to the present invention. A test structure may be investigated by means of microscopy, *e.g.*, optical microscopy and/or electron microscopy, and/or by means of measurements of electric characteristics of the test structure, *e.g.*, the conductivity of an electrical path comprising at least one via and/or at least one trench filled with metal. These investigations may be performed after the completion of a sequence of electroplating, electropolishing and chemical mechanical polishing. Alternatively, a method of forming a

layer of metal on a semiconductor structure according to the present invention may be interrupted to investigate the test structure.

In a method according to the present invention, electroplating and electropolishing need not be performed in the same electrolyte bath as in the embodiments described above. In other embodiments, in the electroplating process, the semiconductor structure is brought into contact with a first electrolyte. Subsequently, the semiconductor structure is removed from the first electrolyte and brought into contact with a second electrolyte. The first and the second electrolyte may differ in the concentration of components like conductor metal ions, acids and/or additives. The first and the second electrolyte may have a different temperature and/or a different conductivity. The electroplating process and the electropolishing process may be performed in plating cells having a different geometrical arrangement of the electrode and the semiconductor structure.

Bringing the semiconductor structure and/or the electrode into contact with an electrolyte need not comprise immersing the semiconductor structure and/or the electrode in the electrolyte. For example, in other embodiments of the present invention, a spray of electrolyte may used.

The particular embodiments disclosed above are illustrative only, as the invention may be modified and practiced in different but equivalent manners apparent to those skilled in the art having the benefit of the teachings herein. For example, the process steps set forth above may be performed in a different order. Furthermore, no limitations are intended to the details of construction or design herein shown, other than as described in the claims below. It is therefore evident that the particular embodiments disclosed above may be altered or modi-

fied and all such variations are considered within the scope and spirit of the invention. Accordingly, the protection sought herein is as set forth in the claims below.